RS2130

2-Axis,±16g,I²S Digital Accelerometer

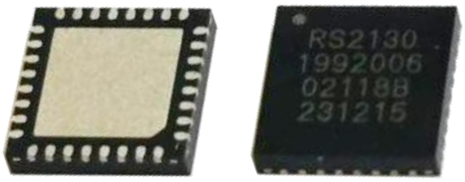
1. FEATURES

- Range: ±2g to ±16g
- Digital output: 48 kHz I²S/TDM/PDM
- High resolution: 14 bits
- Bandwidth: up to 4 kHz
- Low latency: 50 μs typical at 4 kHz bandwidth
- Low noise: 50 μg/√Hz typical for x- and y-axes
- Operating temperature range: -40°C to +125°C
- Package: 5mm × 5mm × 1.2 mm QFN32

2. APPLICATIONS

- RNC active noise control
- Adaptive suspension control

3. OUTLINE



4. GENERAL DESCRIPTION

RS2130 adopts automotive-grade MEMS and ASIC processes, is compatible with mainstream devices, and has the excellent characteristics of high bandwidth, low latency and ultra-low noise, which is well suited for wideband active noise control and high-precision vibration measurement applications.

5. FUNCTIONAL BLOCK DIAGRAM

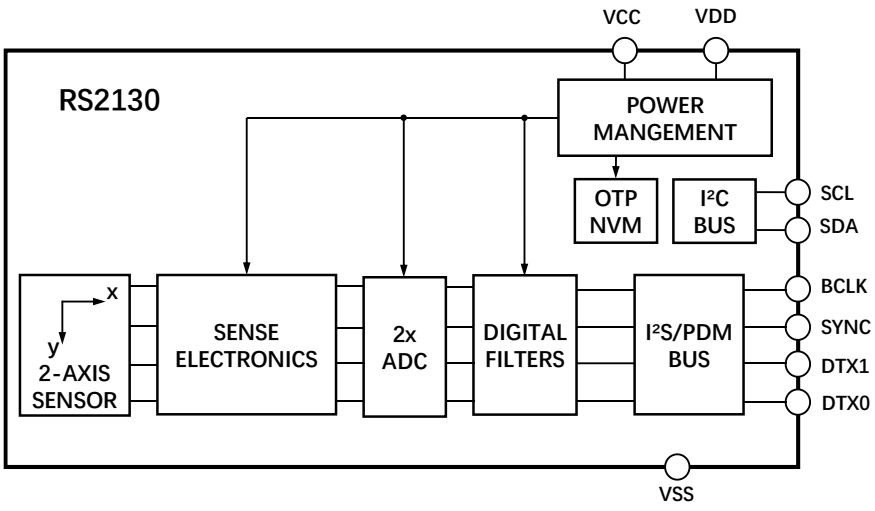


Figure 1. Functional Block Diagram

Content

6. ABSOLUTE MAXIMUM RATINGS

Table 1.

Parameter	Rating
Mechanical Shock （Any Axis, Unpowered）	±4000 g (0.5 ms half sine)
Mechanical Shock （Any Axis, Powered）	±2000 g (0.5 ms half sine)
Supply Voltage	-0.3V to +4V
ESD (HBM)	2000 V
Latch-up Current	100 mA
Storage Temperature Range	-55℃ to +150℃
Operating Temperature Range	-40℃ to +125℃

7. SPECIFICATIONS

TA = 25 °C, VCC = 3.3 V, acceleration = 0 g, nominal clock set to 3.072 MHz, unless otherwise specified.

Table 2. Accelerometer Specifications Part 1

Parameter	Test Conditions/ Comments	Value	Unit
Full-scale Range		±16	g
Nonlinearity	Percentage of full-scale range	±1	% FSR
Cross Axis Sensitivity		±3	%
Sensitivity (@±16g FSR) Sensitivity Change Due to Temperature X- and Y-Axes	−40°C ≤ TA ≤ +25°C and +25°C ≤ TA ≤ +125°C	512 ±2.5	LSB/g %
Resolution		14	Bits
Initial 0 g Output Deviation	Over full operating temperature range	<±200	mg
Frequency Response Cutoff (–3 dB) Frequency	User selectable Filters only	1.5 3 4(default)	kHz
Noise		50	µg/√Hz

Table 2. Accelerometer Specifications Part 2

Parameter	Test Conditions/ Comments	Value	Unit
Self Test Positive Output Change X- and Y-Axes Negative Output Change X- and Y-Axes	 DC self test magnitude DC self test magnitude 	 6.6 -6.6	 g g
Operating Voltage		3.3	V
Regulated Input/Output Voltage		1.8	V
Supply Current		3	mA
Turn On Time		200	µs
I²S/TDM Interface Frame Rate Word Size I²S/TDM2 TDM4 TDM8 Input Clock Frequency I²S/TDM2 TDM4 TDM8	 BCLK from master device 32-bit word size 16-bit word size 32-bit word size 16-bit word size	 48 32 16,32 16 3.072 3.072 6.144 6.144	 kHz Bits Bits Bits MHz MHz MHz MHz
Latency (@4kHz bandwidth)		50	µs

Note: Regulate voltage can't be used as I²C pull-up voltage

8. PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

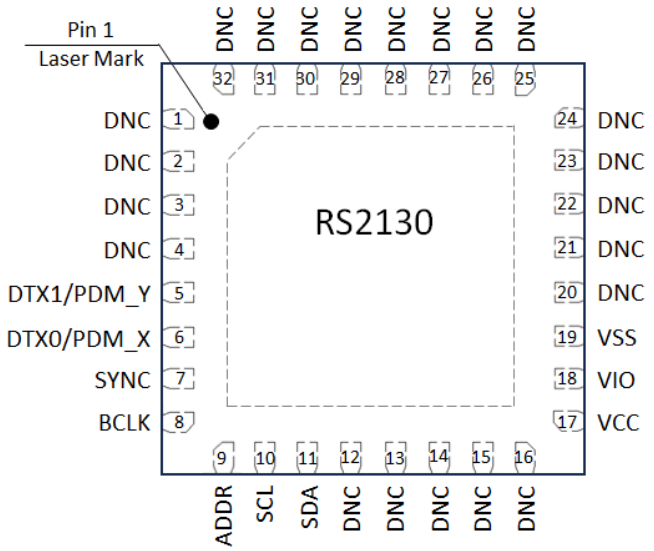


Figure 2. Pin Configuration

Table 3.

Pin No.	Mnemonic	Description
1~4	DNC	Do not connect. Do not connect these pins.
5	DTX1/PDM_Y	I²S Data Channel 1/PDM Y axis output.
6	DTX0/PDM_X	I²S Data Channel 0/PDM X axis output.
7	SYNC	I²S Sync.
8	BCLK	I²S Clock.
9	ADDR	I²C Address Select.
10	SCL	I²C Serial Clock.
11	SDA	I²C Serial Data.
12~16	DNC	Do not connect. Do not connect these pins.
17	VCC	Supply Voltage.
18	VDD/VIO	Internal Regulator Output Voltage.
19	VSS	Reference Voltage. Connect this pin to ground.
20~32	DNC	Do not connect. Do not connect these pins.
	EP	Exposed Pad. The exposed pad must be connected to ground.

9. TYPICAL PERFORMANCE CHARACTERISTICS

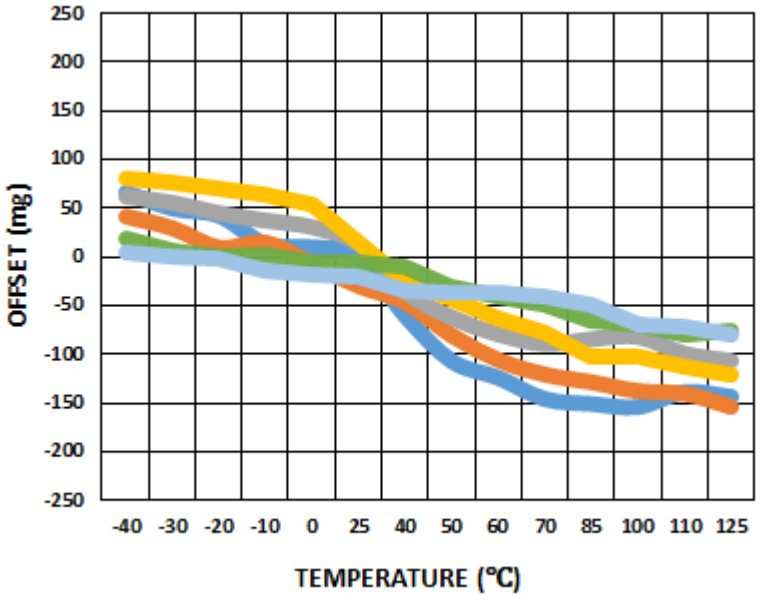


Figure 3. Offset vs. Temperature

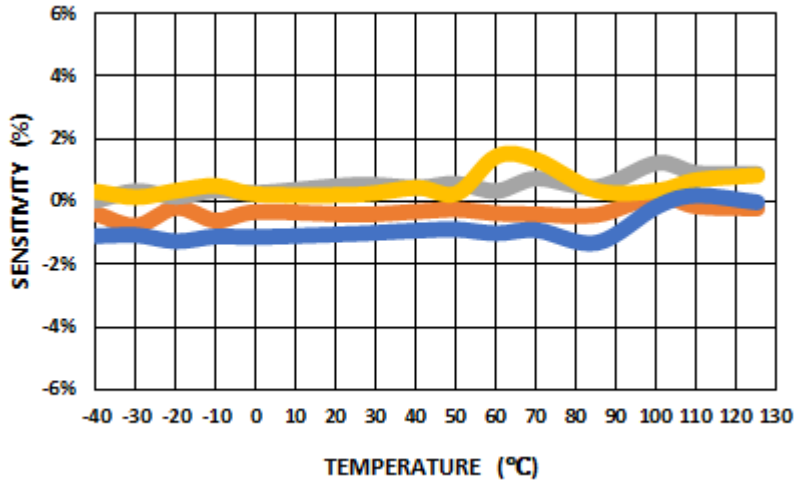


Figure 4. Sensitivity vs. Temperature

10. THEORY OF OPERATION

The RS2130 treats all two sensor channels independently. There are two analog channels in the ASIC die with separate analog signal processing for each accelerometer axis. Each analog channel is then sampled by separate digital signal processing blocks that process the samples for the common communications interface block. Therefore, if one sensor channel fails, transmission of acceleration data continues for the other axes.

11. APPLICATIONS INFORMATION

APPLICATION CIRCUIT

Figure 5 shows the recommended application circuit for the RS2130. The operating power pin, VCC (Pin 17), requires a 100 nF bypass capacitor to ground (VSS, Pin 19) placed as close as possible to the pin. The voltage regulator output pin, VDD (Pin 18), requires a 1 µF capacitor. The two I²C lines, SCL (Pin 10) and SDA (Pin 11), each require a pull-up resistor to VCC. The value of these resistors is dependent on bus capacitance. The exposed pad on the bottom of the package must be connected to ground.

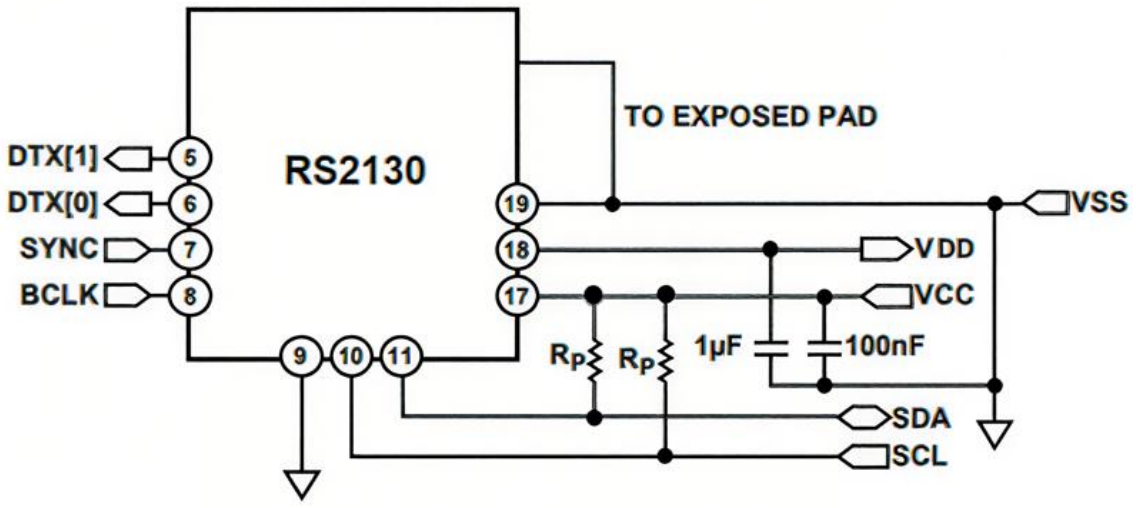


Figure 5. Recommended Application Circuit

POWER

The RS2130 has a single power input pin, VCC, which operates at a nominal voltage of 3.3 V. An internal regulator steps this voltage down to 1.8 V. The VCC pin must be properly bypassed, as shown in Figure 5, to remove ac fluctuations from the power supply.

VDD is the output of the internal voltage regulator, which holds the pin at a constant 1.8 V. This pin must also be decoupled from ac noise for stability. VCC must be used as the pull-up voltage for the I²C lines (SCL and SDA).

INTERFACING WITH A²B TRANSCEIVERS

The RS2130 is designed to interface directly with an I²S capable A²B transceiver. The connection between the RS2130 and the A²B transceiver is shown in Figure 6. A generic A²B transceiver can be used. Refer to the appropriate transceiver data sheet for additional details.

Power

The RS2130 operates as a phantom powered slave device and, therefore, must derive power directly from the A²B transceiver. Connect one of the VOUT pins (3.3 V) from the transceiver to VCC on the RS2130, being sure to properly decouple the supply on both ends.

Communications

Directly connect the BCLK pin and the SYNC pin between the RS2130 and the A²B transceiver. The DTX1 and DTX0 pins on the RS2130 are outputs (data transmit) and must be connected to the corresponding DRX0 and DRX1 (data receive) pins on the transceiver. Adding small (~100 Ω) series resistors to these four lines may improve electromagnetic interference (EMI) performance. The exact value of these resistors depends on the observed EMI characteristics of the system. SCL and SDA must also be connected directly between the two devices, taking care to choose appropriate pull-up resistors. Use VCC as the pull-up voltage for I²C.

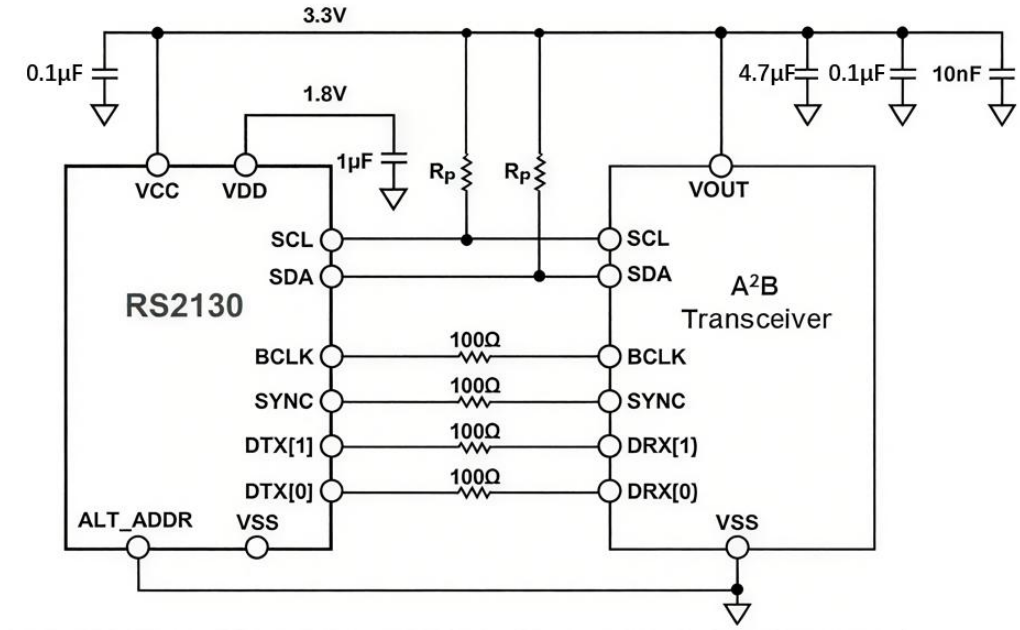


Figure 6. RS2130 to A²B Transceiver Connection Diagram

USING SELF TEST

The sensor self test is a diagnostic test. In this test, the sensor proof mass is deflected by an electrostatic force, thereby creating a measurable output change. For a self test routine to be evaluated properly, the change in output must be measured before and after applying the self test force. If this change is within the specified values shown in Table 2, it is considered successful. The RS2130 features positive and negative self test routines.

The RS2130 features a flexible self test routine to evaluate the condition of the sensors. Self test can be activated in following modes:

- Positive self test mode. In this mode, a positive dc excitation is applied to the sensor along the desired axis. This excitation is approximately 6.6 g for the x- and y-axes, plus any excitation from the environment.
- Negative self test mode. In this mode, a negative dc excitation is applied to the sensor along the desired axis. This excitation is approximately −6.6 g for the x- and y-axes, plus any excitation from the environment.

When first powering on the RS2130, the user must use the positive and negative dc self test to achieve an accurate understanding of device health. Each axis is capable of controlling its self test independently of the other axes, resulting in many combinations of self test settings. These settings are configured in the X_ST and Y_ST registers and the corresponding EN_ST_X and ST_ POL_ X bits.

The mapping of all possible settings of these bits and the resultant self test force is shown in Table 4.

Table 4. Self Test Settings Combinations

EN_ST_X	ST_ POL_ X	Self Test Force
0	0	Self test is disabled
0	1	Self test is disabled
1	0	Positive self test
1	1	Negative self test

When a self test force is exerted along any axis, the value returned from the sensor is additive with any external force applied to the accelerometer.

For simplicity, assume all axes receive the same input. The resultant measurement returned from the RS2130 after applying self test is the sine wave added to the self test excitation.

Be sure to account for gravity in self test measurements.

Taking an accurate self test measurement involves a few steps. For the two dc self test modes, the following routine must be followed to accurately assess the results of self test:

1. Ensure all self test functionality is disabled. That is, set the X_ST and Y_ST registers (Address 0x5E) to 0x00.
2. Read acceleration data for the x-axis. It is recommended to take an average of 25 ms to reduce the influence of noise in the measurement.
3. Deactivate self test by asserting the X_ST bit and wait for the output to transition to the maximum value.
4. Read acceleration data again for 25 ms.
5. Subtract the data collected in Step 2 from the data collected in Step 4 to determine the magnitude of the positive self test delta (STΔ).
6. Deactivate the ST_ POL_ X bit, and wait for the output to transition to the minimum value.
7. Read acceleration data again for 25 ms.
8. Subtract the data collected in Step 2 from the data collected in Step 7 to determine the magnitude of the negative self test delta (STΔ).
9. Compare the positive and negative STΔ magnitudes to the limits in Table 2. If both magnitudes are within the minimum and maximum specifications, the device passed the self test. Otherwise, the device failed and must be flagged for further investigation.
10. Repeat Step 1 to Step 9 for the y-axis, sequentially.

Self test must be activated one channel at a time, meaning that Step 1 to Step 9 must be repeated for the x-, y-axis channels, sequentially.

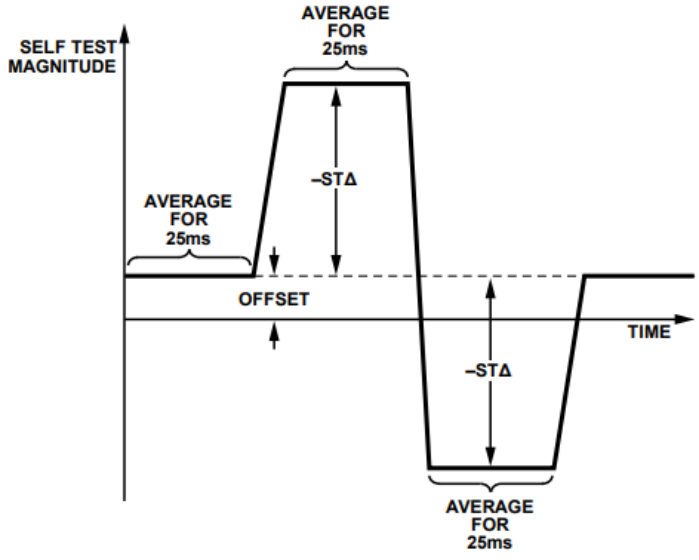


Figure 7. DC Self Test Measurement

12. SERIAL COMMUNICATIONS

The RS2130 communicates via both 4-wire I²S and 2-wire I²C digital communication interfaces. The I²S bus is the primary means of outputting data, and the I²C bus configures the register settings. In both cases, the RS2130 operates as a slave device, receiving commands and responding with requested data. These two ports operate independently and use separate pins. Therefore, these ports can be used simultaneously.

I²S/TDM INTERFACE

The RS2130 constantly streams data out of the I²S port. This protocol is suitable for obtaining high speed, synchronous accelerometer data. The RS2130 operates at a clock speed of 3.072 MHz (typical) or 6.144 MHz with a frame frequency of 48 kHz. The device supports 16-bit TDM4 and TDM8, as well as 32-bit I²S/TDM2 and TDM4.

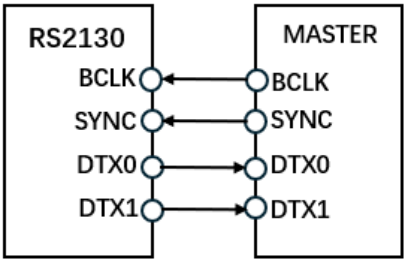


Figure 8. I²S/TDM Wiring Diagram

Signals

The RS2130 uses 4-wire I²S interface, comprising one continuous serial clock, one synchronization signal, and two serial data channels. There are numerous naming conventions for these channels. The RS2130 uses the same terminology and symbols as the A²B family of transceivers. See Table 5 for a comparison of the names used in the I²S specification against the names used in the RS2130.

Table 5. I²S Signal Names

I²S Specification		RS2130	
Full Name	**Symbol**	**Full Name**	**Symbol**
Continuous Serial Clock	SCK	Bit Clock	BCLK
World Select	WS	Sync	SYNC
Serial Data	SD	Data Transmit	DTX

Bit Clock (BCLK)

The bit clock (BCLK) line controls the timing of transactions between the master (A²B transceiver or other controller) and slave (RS2130). This clock must be supplied externally to the BCLK pin (Pin 8) at a rate of either 3.072 MHz or 6.144MHz. The incoming clock frequency must be specified in the CLOCK_RATE register (Address 0x2B).

The RS2130 has no internal clock, and all timing is derived from BCLK. BCLK must be running at all times for the RS2130 to operate, even when using I²C to read and/or write registers.

Sync (SYNC) Signal

The SYNC line selects the channel being transmitted. By default, with SYNC high (set to 1), the right channel is transmitting. With SYNC low (set to 0), the left channel is transmitting (in TDM2 mode). This behavior can be reversed by asserting the INV bit in the I²S_CFG0 register (Address 0x2A). SYNC demarcates the boundary between the first and second halves of the frame.

The value of SYNC is latched on the rising edge of BCLK as long as INV (Address 0x2B, Bit 2) = 0. After SYNC changes value, the timing of the transmission of the MSB of the data depends on the value of the early bit in the I²S_CFG0 register. If early = 0, the SYNC pin changes in the same cycle as the MSB of the first data channel. If early = 1, the SYNC pin changes one cycle before the MSB of the first data channel.

By default, the SYNC pin changes value on the rising edge of BCLK. This change can be altered to occur on the falling edge by asserting the BCLK_INV bit in the I²S_CFG1 register.

Data Transmit (DTX) Signal

The data transmit (DTX) lines send data from the RS2130 to the master device. Data is transmitted in twos complement format with the most significant bit (MSB) first. The position of the LSB in the transaction is dependent on the word length, as defined in the Packet Format section.

Data can be sent over one or both of the DTX pins, depending on the values of the TX0EN and TX1EN bits in the I²S_CFG1 register, as well as the operating mode.

Packet Format

The RS2130 features four packet formats, depending on the input clock (BCLK) frequency and system requirements. At 3.072 MHz, 32-bit I²S/TDM2 and 16-bit TDM4 are supported. At 6.144MHz, 32-bit TDM4 and 16-bit TDM8 are supported. Note that 32-bit I²S/TDM2 mode requires two data pins, whereas the other mode require only one.

Table 6. Required BCLK Frequencies for All Supported Output Formats

Output Format	16-Bit Mode BCLK Frequency	32-Bit Mode BCLK Frequency	No. of Pins
I²S/TDM2	Not applicable	3.072 MHz	2
TDM4	3.072 MHz	6.144 MHz	1
TDM8	6.144 MHz	Not applicable	1

In I²S/TDM2 mode, the DTX0 pin transmits data from the x- and y-axes. BCLK must be running at 3.072 MHz, and each axis comprises 32 bits.

In TDM4 mode, data from all axes is sent over a single pin, whereas the other pin remains at zero during the entire transaction. Each axis comprises 16 bits with BCLK running at 3.072 MHz and 32 bits at 6.144MHz.

In TDM8 mode, the frame is further divided in eight segments. The first three segments on one pin contain data from all axes, and the remaining segments are held at zero. BCLK must be running at 6.144 MHz, and each axis comprises 16 bits.

The frame rate for all transactions is 48 kHz, which translates to 64 clock cycles at 3.072 MHz or 128 cycles at 6.144 MHz. The number of channels in each frame is always a power of two (two, four, or eight). The RS2130 has two channels, one for each axis. Therefore, one channel beyond the second are set entirely to 0. Table 7 and Table 8 shows how these channels align within each frame, and Figure show how the various I²S configuration settings affect the timing of each transaction. Note that these figures are not to scale, and clock rates differ.

Table 7. Two-Pin I²S/TDM2 Packet Format (3.072 MHz BCLK, 32-Bit Data, TX0EN = 1, TX1EN = 1)

DTX0	DTX1
X-axis data (32-bit) Y-axis data (32-bit)	0x00000000 0x00000000

Table 8. One-Pin TDM4 Packet Format (3.072 MHz BCLK, 16-Bit Data, TX0EN = 1, TX1EN = 0)

DTX0	DTX1
X-axis data (16-bit) Y-axis data (16-bit) 0x0000 0x0000	0x0000 0x0000 0x0000 0x0000

Table 9. One-Pin TDM4 Packet Format (6.144 MHz BCLK, 32-Bit Data, TX0EN = 1, TX1EN = 0)

DTX0	DTX1
X-axis data (32-bit) Y-axis data (32-bit) 0x0000 0x0000	0x0000 0x0000 0x0000 0x0000

Table 10. One-Pin TDM8 Packet Format (6.144 MHz BCLK, 16-Bit Data, TX0EN = 1, TX1EN = 0)

DTX0	DTX1
X-axis data (16-bit) Y-axis data (16-bit) 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000	0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000

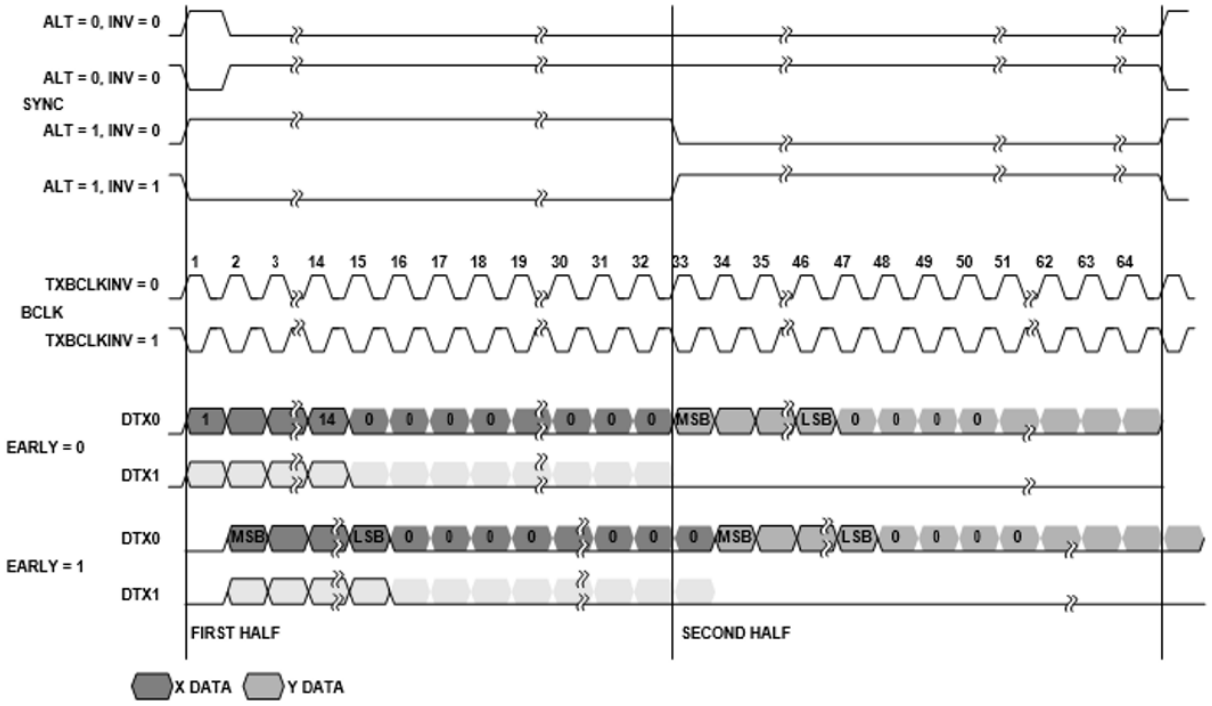


Figure 9. 3.072 MHz I²S/TDM2 Timing (32-Bit Data)

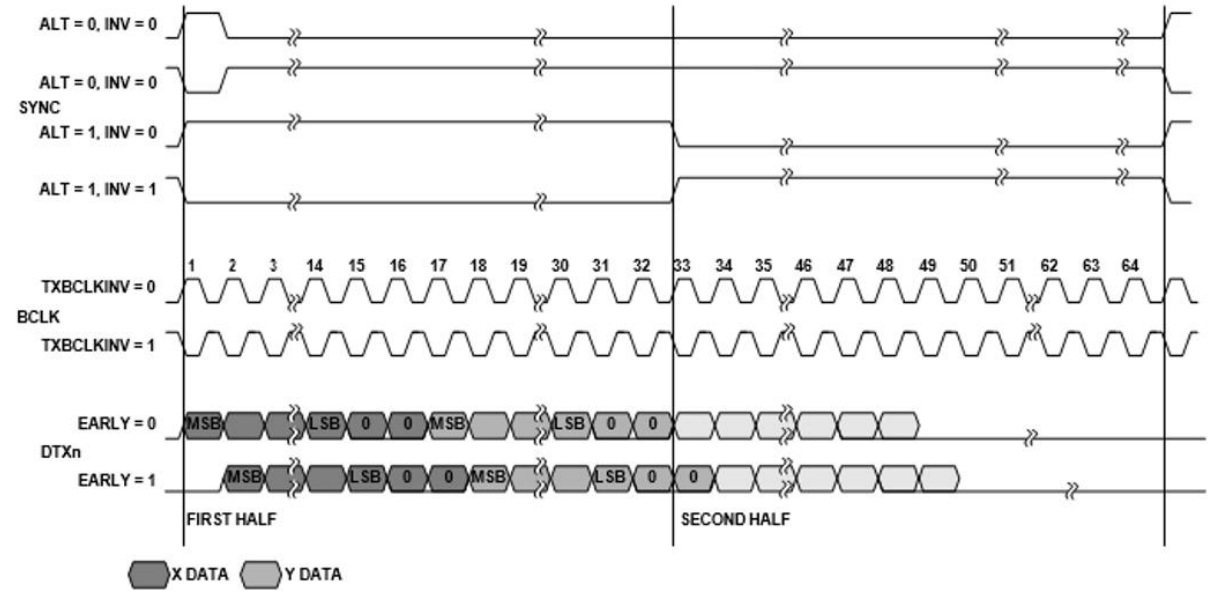


Figure 10. 3.072 MHz TDM4 Timing (16-Bit Data)

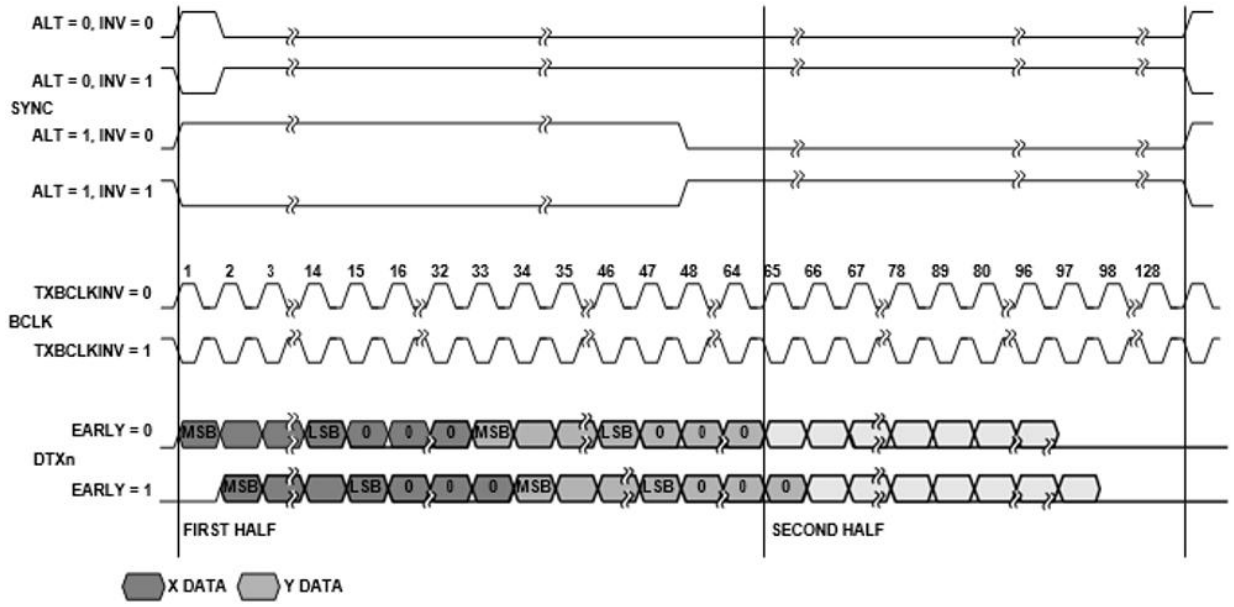


Figure 11. 6.144 MHz TDM4 Timing (32-Bit Data)

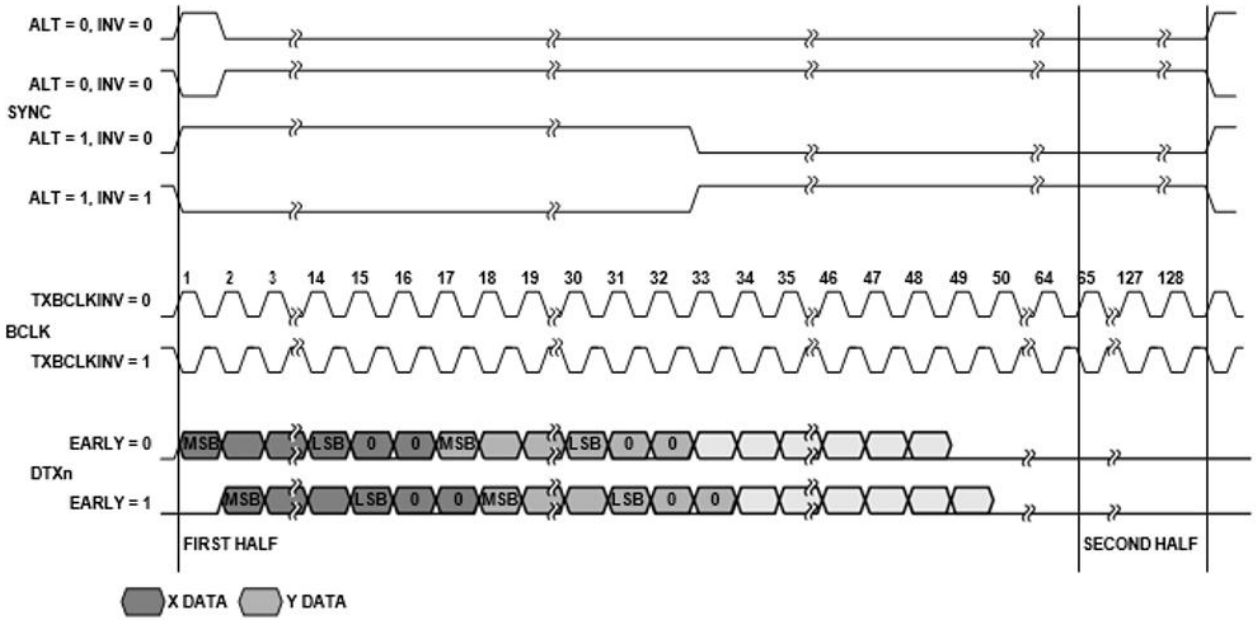


Figure 12. 6.144 MHz TDM8 Timing (16-Bit Data)

I²C INTERFACE

The I²C interface of RS2130 is a slave bus. There are two signals associated with the I²C bus: the serial clock SCL and serial data SDA. The SDA is a bi-directional line used to send or receive data from the interface. Both lines must be connected to VCC through external pull-up resistors.

The default I²C address of RS2130 is 0b1010011. It is used if the ADDR pin is pulled to 'GND'. The alternative address 0b0011101 is selected by pulling ADDR to 'VCC'.

The I²C bus is implemented with both fast mode (400 kHz) and standard mode.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver then must pull the SDA line 'low' so it remains low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The transaction begins with a start (ST) condition generated by master, followed by 7 bits slave address (SAD) and 1 read/write bit, then the master sends the one byte register address (RAD). If it is a read operation, a repeated start (SR) condition must be issued after the register address byte. If it is a write operation, the master will transmit data which will be written into the register addressed by register address byte. The slave sends out slave acknowledge condition (ACK) after the slave address issued by master matches its slave address, and after master sends out register address and receives data byte written by master. The master must assert master acknowledge condition (MACK) after receives data from slave.

Data are transferred in byte format with MSB sent out first. The number of bytes transferred is unlimited until no master acknowledge (MNACK) condition asserted by master for read operation, or when master issues stop condition for write operation.

Table 11. I²C Single Byte Write

Master	ST	SAD+W		RADR		DATA		SP
Slave			ACK		ACK		ACK	

Table 12. I²C Single Byte Read

Master	ST	SAD+W		RADR		RS	SAD+R			MNACK	SP
Slave			ACK		ACK			ACK	DATA		

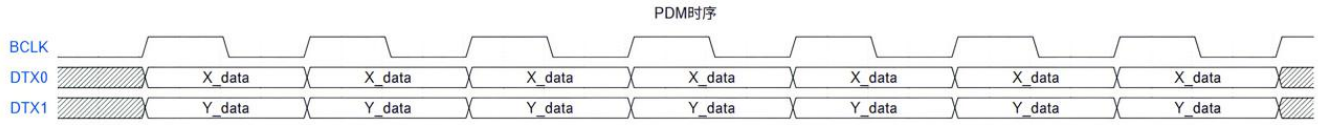
Table 13. I²C Multiple Byte Write

Master	ST	SAD+W		RADR		DATA		DATA		SP
Slave			ACK		ACK		ACK		ACK	

Table 14. I²C Multiple Byte Read

Master	ST	SAD+W		RADR		RS	SAD+R			MACK		MNACK	SP
Slave			ACK		ACK			ACK	DATA		DATA		

Table 15.PDM Timing



13. REGISTER MAP

Table 16. Register Summary

Addr.	Name	Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default	RW
0x00	VERID	[7:0]	Revision ID								0x21	R
0x03	X_DATA_LO	[7:0]	X_DATA[5:0]						NA		N/A	R
0x04	X_DATA_HI	[7:0]	X_DATA[13:6]								N/A	R
0x05	Y_DATA_LO	[7:0]	Y_DATA[5:0]						NA		N/A	R
0x06	Y_DATA_HI	[7:0]	Y_DATA[13:6]								N/A	R
0x0F	CHIPID	[7:0]	CHIPID								0xB1	R
0x13	CONFIG	[7:0]	Reserved						Y_axis _EN	X_axis _EN	0	R/W
0x14	Range	[7:0]			Range						0	R/W
0x1C	X_filter	[7:0]						LPF_X_EN	LPF_X		0	R/W
0x1D	Y_filter	[7:0]						LPF_Y_EN	LPF_Y		0	R/W
0x2A	I²S_CFG0	[7:0]	SYNC_ INV	SYNC_ EARLY	SYNC_ ALT	SLOT_ SIZE		TDM_I2S	TDM_MODE		0	R/W
0x2B	I²S_CFG1	[7:0]	CLK_ RATE	Reserved				BCLK_ INV	TX1_ EN	TX0_ EN	0	R/W
0x2C	PDM_EN	[7:0]	Reserved						PDM_ EN_Y	PDM_ EN_X	0	R/W
ODB5E	ST_XY	[7:0]			EN_S T_Y	EN_S T_X	EN_HIZ _DTX		ST_P OL_Y	ST_P OL_X	0	R/W

* N/A means not applicable.

14. REGISTER DETAILS

DEVICE ID REGISTERS

The device ID registers contain the information necessary to identify the specific version of the RS2130 device.

Table 17. VERID Register Summary (Address: 0x00, Name: VERID, Default: 0x21)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	VERID	0x21…0x0f	This field contains the revision ID for this product. This field identifies each major revision of the RS2130, beginning with 0 and incrementing for each significant change.	0x21	R

VERID contains the customer revision ID for the RS2130. This field is intended to store significant changes to the device revision throughout its lifetime.

CONFIG REGISTERS

Table 18. CONFIG Register Summary (Address: 0x13, Name: CONFIG)

Bits	Bit Name	Settings	Description	Default	Access
[1]	Y_axis_EN		Y_axis enable	0	RW
		0	Y axis is disabled		
		1	Y axis is enabled		
[0]	X_axis_EN		X_axis enable	0	RW
		0	X axis is disabled		
		1	X axis is enabled		

RANGE REGISTERS

Table 19. RANGE Register Summary (Address: 0x14, Name: RANGE)

Bits	Bit Name	Settings	Description	Default	Access
[5:3]	RANGE		RANGE SECLET	0	RW
		000	1g		
		001	2g		
		010	4g		
		011	8g		
		100	16g		

FILTER REGISTERS

Table 20. Filter_X Register Summary (Address: 0x1C, Name: Filter_X)

Bits	Bit Name	Settings	Description	Default	Access
[2]	LPF_X_EN		LPF_X_EN	0	RW
		0	disabled (default 4k)		
		1	enabled		
[1:0]	LPF_X		X_axis enable	0	RW
		10	3KHz		
		11	1.5KHz		

Table 21. Filter_Y Register Summary (Address: 0x1D, Name: Filter_Y)

Bits	Bit Name	Settings	Description	Default	Access
[2]	LPF_Y_EN		LPF_Y_EN	0	RW
		0	disabled (default 4k)		
		1	enabled		
[1:0]	LPF_Y		Y_axis enable	0	RW
		10	3KHz		
		11	1.5KHz		

I²S CONFIGURATION REGISTERS

The I²S configuration registers control various settings for the I²S bus of the RS2130. For more information about how these settings affect the timing of the I²S output, see the I²S/TDM Interface section.

Table 22. I²S_CFG0 Register Summary (Address: 0x2A, Name: I²S_CFG0)

Bits	Bit Name	Settings	Description	Default	Access
[7]	SYNC_INV		I²S Clock Polarity. This bit sets the clock polarity for I²S communications.	0	RW
		0	Audio frame begins on rising edge of SYNC signal.		
		1	Audio frame begins on falling edge of SYNC signal.		
[6]	SYNC_INV		I²S Early Sync. This bit sets the timing of the SYNC signal.	0	RW
		0	SYNC changes in same cycle as the MSB of the first data channel.		
		1	SYNC changes one cycle before the MSB of the first data channel.		
[5]	SYNC_ALT		I²S Alternating Sync. This bit sets the behavior of the SYNC signal.	0	RW
		0	SYNC is asserted for one BCLK cycle only.		
		1	SYNC is asserted at the beginning of each sampling period and then toggled in the middle of each sampling period.		
[4]	SLOT_SIZE		I²S/TDM Slot Size. This bit sets the size for each TDM slot.	0	RW
		0	Each slot transmits 32 bits of data.		
		1	Each slot transmits 16 bits of data.		
[2]	I2S/TDM		I²S/TDM mode select		
		0	I²S mode		
		1	TDM mode		
[1:0]	TDM_MODE		I²S/TDM Mode. This field sets the TDM mode for I²S communications.	0	RW
		00	TDM2.		
		01	TDM4.		
		11	TDM8		

Table 23. I²S_CFG1 Register Summary (Address: 0x2B, Name: I²S_CFG1)

Bits	Bit Name	Settings	Description	Default	Access
[7]	CLK_RATE		A²B Clock Rate Select. This field sets the rate of the BCLK signal. Supplying a clock that does not match the setting in this field may result in unpredictable behavior and incorrect data.	0	RW
		0	6.144MHz		
		1	3.072 MHz		
[2]	BCLK_INV		I²S Transmit Clock Inversion. This bit sets the edge of BCLK on which the data transmit pins change.	0	RW
		0	DTX0 and DTX1 pins change on the rising edge of BCLK.		
		1	DTX0 and DTX1 pins change on the falling edge of BCLK.		
[1]	TX1_EN		I²S Channel 1 Enable. This bit enables the transmission of data on I²S Channel 1 (DTX1).	0	RW
		0	Data transmission is disabled on Channel 1.		
		1	Data transmission is enabled on Channel 1.		
[0]	TX0_EN		I²S Channel 0 Enable. This bit enables the transmission of data on I²S Channel 0 (DTX0).	0	RW
		0	Data transmission is disabled on Channel 0.		
		1	Data transmission is enabled on Channel 0.		

PDM CONFIGURATION REGISTERS

Table 24. PDM Register Summary (Address: 0x2C, Name: PDM)

Bits	Bit Name	Settings	Description	Default	Access
[1]	PDM_EN_Y		PDM y-axis enable	0	RW
		0	Disable y-axis PDM output		
		1	Enable y-axis PDM output		
[0]	PDM_EN_X		PDM x-axis enable	0	RW
		0	Disable x-axis PDM output		
		1	Enable x-axis PDM output		

X-AXIS SELF TEST CONFIGURATION REGISTER

The x-axis self test configuration register enables the self test functionality on the x-axis. Although the RS2130 supports two types of self test on each axis (negative, positive), only one such test can be enabled at one time. See Table 4 for a list of all possible combinations of settings for this register and how they affect the self test output. See the Using Self Test section for more information.

Table 25. X_ST Register Summary (Address: 0x5E, Name: X_ST)

Bits	Bit Name	Settings	Description	Default	Access
[4]	EN_ST_X		X-Axis Self Test Enable. This bit enables the self test functionality on the x-axis.	0	RW
		0	Self test is disabled on the x-axis.		
		1	Self test is enabled on the x-axis.		
[0]	ST_POLAR_X		X-Axis Positive or Negative Self Test select ctrl. This bit choose Positive or Negative Self test on the x-axis.	0	RW
		0	A positive self test is applied to the x-axis.		
		1	A negative self test is applied to the x-axis.		

Y-AXIS SELF TEST CONFIGURATION REGISTER

The y-axis self test configuration register enables self test functionality on the y-axis. Although the RS2130 supports two types of self test on each axis (negative, positive), only one such test can be enabled at a time. See Table 4 for a list of all possible combinations of settings for this register and how they affect the self test output. See the Using Self Test section for more information.

Table 26. Y_ST Register Summary (Address: 0x5E, Name: Y_ST)

Bits	Bit Name	Settings	Description	Default	Access
[5]	EN_ST_Y		Y-Axis Self Test Enable. This bit enables the self test functionality on the y-axis.	0	RW
		0	Self test is disabled on the y-axis.		
		1	Self test is enabled on the y-axis.		
[1]	ST_POLAR_Y		Y-Axis Positive or Negative Self Test select ctrl. This bit choose Positive or Negative Self test on the y-axis.	0	RW
		0	A positive self test is applied to the y-axis.		
		1	A negative self test is applied to the y-axis.		

X-AXIS ACCELEROMETER DATA REGISTERS

The x-axis accelerometer data registers contain the 14-bit, zero padded, x-axis acceleration data. X_DATA_LO contains the 6 LSBs, and X_DATA_HI contains the 8 MSBs. The 14-bit acceleration value is left justified, with Bit 0 and Bit 1 in the X_DATA_LO register fixed at 0. This setup mimics the format for 16-bit I²S data.

Table 27. X_DATA_LO Register Summary (Address: 0x03, Name: X_DATA_LO)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LSB	0	0

Table 28. X_DATA_HI Register Summary (Address: 0x04, Name: X_DATA_HI)

B7	B6	B5	B4	B3	B2	B1	B0
MSB	0	0	0	0	0	0	0

Y-AXIS ACCELEROMETER DATA REGISTERS

DATA REGISTERS The y-axis accelerometer data registers contain the 14-bit, zero padded y-axis acceleration data. Y_DATA_LO contains the 6 LSBs, and Y_DATA_HI contains the 8 MSBs. The 14-bit acceleration value is left justified, with Bit 0 and Bit 1 in the Y_DATA_LO register fixed at 0. This setup mimics the format for 16-bit I²S data.

Table 29. Y_DATA_LO Register Summary (Address: 0x05, Name: Y_DATA_LO)

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	LSB	0	0

Table 30. Y_DATA_HI Register Summary (Address: 0x06, Name: X_DATA_HI)

B7	B6	B5	B4	B3	B2	B1	B0
MSB	0	0	0	0	0	0	0

15. AXES OF ACCELERATION SENSITIVITY

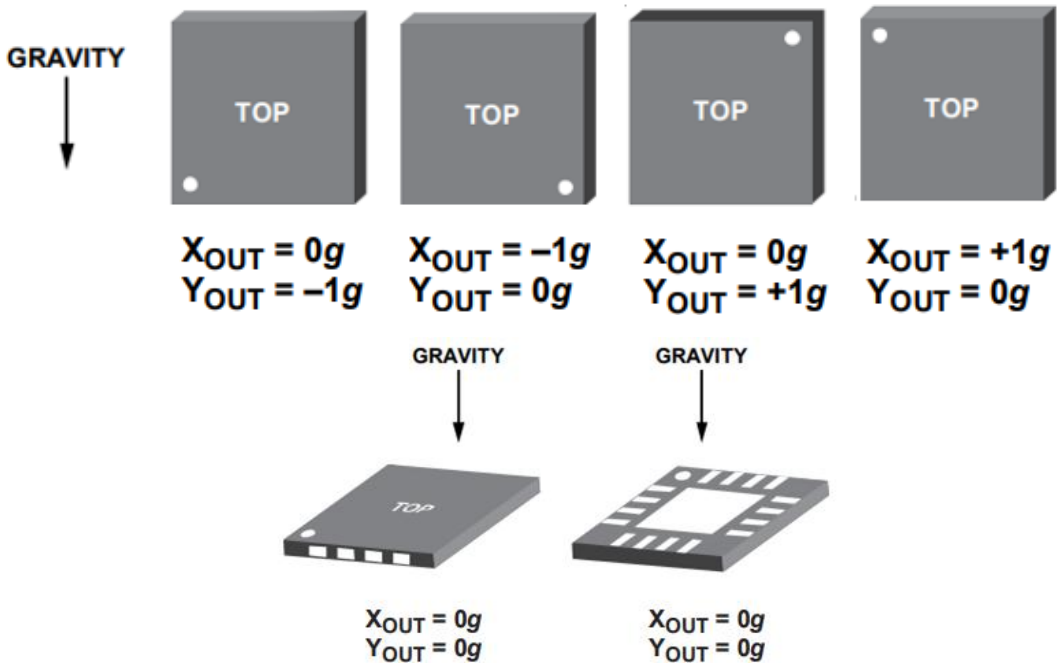


Figure 13. Output Response vs. Orientation to Gravity

16. PACKAGE DIMENSIONS

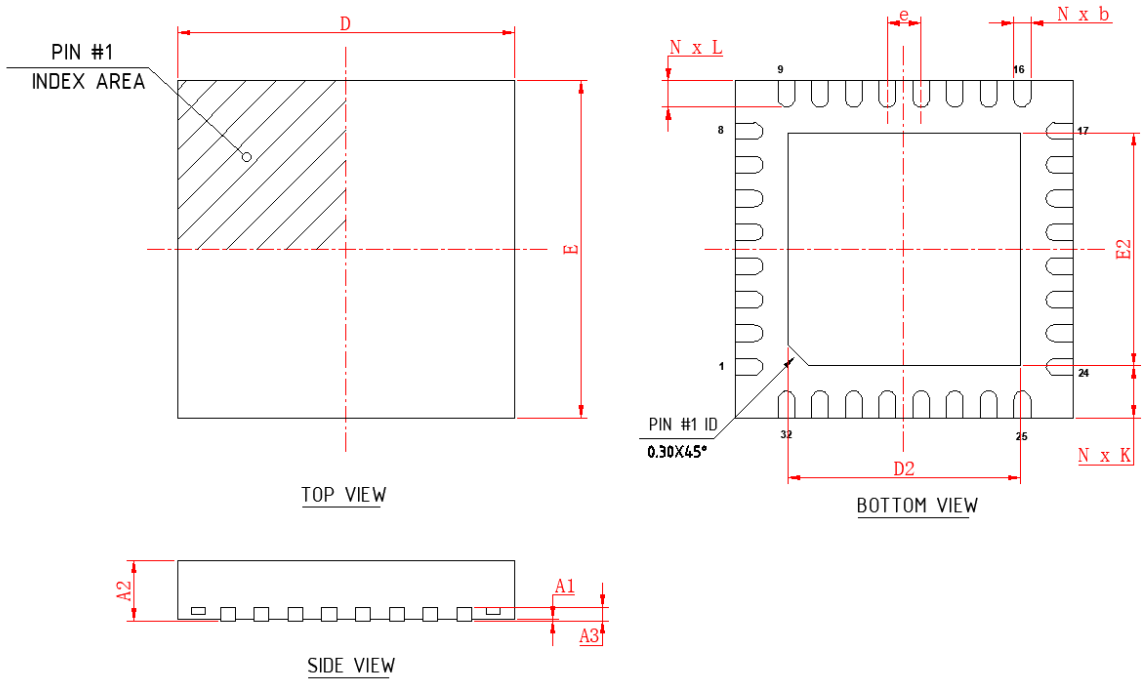


Figure 14. 32-Lead Frame Chip Scale Package

Table 31

Symbol	Min	Mid	Max
A1	0.00	0.02	0.05
A2	1.1	1.2	1.3
A3		0.20 REF	
b	0.18	0.25	0.30
D	4.95	5.00	5.05
E	4.95	5.00	5.05
e		0.50BSC	
D2	3.30	3.45	3.55
E2	3.30	3.45	3.55
K		0.20 REF	
L	0.30	0.40	0.50
N		32	

Note:

1. All dimensions are in mm.
2. The dimension is influenced by the molding film. Since it is impossible to predict the local film stretch condition, the values here should be considered as “Target” only.